REMARKS

The Examiner has rejected Claims 23-28 under 35 U.S.C. 112 for lack of antecedent basis for the term "the manageability system interconnect" in lines 29-30 of the independent claims 23 and 26; claims 24-25 and 27-28 were rejected as dependent upon a rejected base claim.

The Examiner has also rejected claims 23-28 as unpatentable under 35 U.S.C. 103 over U.S. Patent 6,834,340 to Lee (hereinafter Lee) in view of U.S. Patent Publication 2002/0091807 to Goodman (hereinafter Goodman). The Examiner has rejected claim 24 and 27 as unpatentable under 35 U.S.C. 103 over U.S. Patent 6,834,340 to Lee (hereinafter Lee) in view of U.S. Patent Publication 2002/0091807 to Goodman (hereinafter Goodman) in further view of U.S. Patent 6665813 to Forsman, et. al. (hereinafter Forsman).

The New Claims

New claims 29-31 correspond to former claims 23-25, but have been rewritten to more clearly recite the contents of each cell and clarify the level of system to which the present application applies.

The Amended Claims

Claim 23 and 26 have been amended to replace the term "manageabilty system interconnect" with the "management interconnect" introduced in the fifth line of the claim. Claims 24-25 and 27-28 are dependent upon claims 23 and 26 respectively. Applicant believes that the amended claims overcome the 35 U.S.C. 112 rejection by providing proper antecedent basis.

The 35 U.S.C. 103 Rejections

Lee Fails to Disclose a Cellular Machine

The Examiner relied upon Lee for elements of a cellular computer system having management interconnect, high speed interconnect, and a first and second cells

each comprising at least one processor, memory, nonvolatile memory, and an interface to the high speed interconnect.

Applicant's claims are drawn to the hardware level of a computer system. Applicant's processors, management processors, memories, nonvolatile memories, and interconnect interfaces are physical functional units implemented in one or more integrated circuits; these integrated circuits are mounted in a module that is a cell.

Upon inspection of Lee, Applicant finds that Lee describes three levels of a computer system architecture, a hardware level best illustrated by Lee's FIG 1, providing an environment for a first level virtual-machine having a pool of resources illustrated in Lee's FIG 2, and a partitioned virtual-machine level illustrated in Lee's FIG 3.

At the hardware level, as illustrated in Lee's FIG 1, Lee provides what appears to be a single management processor (Lee "service processor" 135), having a memory (Lee 191) and coupled to a single nonvolatile memory (Lee 192). It should be noted that Lee therefore **fails to provide separate hardware-level management processors for each cell as claimed**.

The second level of Lee, illustrated in Lee's FIG 2, is the level cited by the examiner for the element of cells. Lee's FIG 2, however, merely discloses a puddle having a single nonvolatile memory (Lee 298), several processors (Lee 232-238), several memories (240-246), and several I/O adapters (Lee 248-262), loosely attached through a firmware "hypervisor" (Lee 212) to "operating systems" (Lee 202-208). Lee then describes allocation of these resources to the various operating systems with reference to his FIG 3. The management processor (Lee 135) is not mentioned with reference to Lee's FIG 2, nor is any mention made of management interconnect between the multiple management processors of the claimed invention. There is only a bald statement that this second level virtualizes the underlying architecture, with its singular NVRAM

Only at the partitioned virtual-machine level illustrated in Lee's FIG 3 does an association of data structures (Lee 312), interfaces, and "firmware" communicating with "working areas" in system memory appear. No mention of processors is made at this level. Even assuming that these virtual-level associations provided cells with processors and memory communicating with each other, **there is no mention of**

management interconnect, separate management processors or separate nonvolatile firmware memories at this virtual level. While Lee defines firmware as having been stored in a nonvolatile memory at some point, there is no clue as to whether Lee's "hypervisor" firmware and partition-specific firmware executes on a primary processor or on the solitary management processor; nor does Lee state whether the firmware is copied to RAM or executed from the single NVRAM. While Lee states that firmware update request can be initiated by an "RTAS call", and carried out by the management processor, the management processor remains singular.

The system of Lee is therefore NOT a cellular system with cell-specific management processors and nonvolatile memory as claimed at either the hardware or virtual-machine levels. Even if it were a cellular system at the partitioned virtual-machine level, this is not analogous to the hardware-level system claimed.

Goodman Provides Only Part of Elements Missing in Lee

The system of Goodman provides a cellular system at the hardware level having many elements analogous to elements of the claims. Goodman provides cells having processors, memory, and interface to high-speed interconnect. These cells, however, lack cell-specific management processors and management interconnect as was explained in the response to the first office action.

The Combination Fails to Provide Essential Claim Elements

Even were the examiner to rewrite his rejection to rely on the system of Goodman for cellular organization, while grafting on the management processor and management interconnect of Lee, that combination also fails to meet the Examiner's burden for a 35 U.S.C. 103 rejection, because the combination lacks the cell-specific management processors and management interconnect claimed.

Further, such a combination would fail to provide the element of transmitting update firmware over the management interconnect from one cell to another cell.

Lee Teaches Away From the Combination

The system of Lee teaches away from the system claimed by disclosing a single nonvolatile memory (Lee 192, 298), therefore Lee can not be combined with

Goodman to create the claimed invention – because the claimed invention provides the function, taught by neither Lee nor Goodman, of updating one nonvolatile memory from another nonvolatile memory of another cell of the *same system*. Even at the virtual machine level of FIG 3, Lee teaches away by suggesting that the firmware of each partition be different.

The 35 U.S.C. 103 Rejection Does Not Meet The Required Standard

Since elements recited by claims do not in fact exist in the art cited by the Examiner; the Examiner has failed to meet his burden. For a valid 35 U.S.C. rejection, an Examiner must showing existence of the elements in the cited references, together with a suggestion that the elements be combined to produce the claimed invention.

Dependent Claims 24, 27

While Forsman does teach the use of a cyclic redundancy check to determine whether firmware is corrupt, Forsman teaches specifically that only one copy of much of a machine's firmware (Forsman's composite code) need reside on a machine. When the composite code is corrupt, Forsman looks to a "fresh" copy of firmware from a floppy or from a backup location on a network.

Forsman thereby teaches away from the present invention by teaching that only one copy of firmware need reside in nonvolatile memory on the machine, and therefore teaching that the "fresh" firmware would not reside in nonvolatile memory elsewhere in the same system. In contrast, Applicant's claimed system has the "fresh" copy residing in another cell of the same system.

CONCLUSION

Since the cited combination lacks many elements of the claims, and since Forsman and Lee teach away from the combination, Applicant believes that the pending 35 U.S.C. 103 rejection of independent claim 21 has not met the Examiner's burden of both finding the elements of the claimed invention in the art and a suggestion in the art that these elements be combined to produce the invention.

Applicant therefore respectfully requests that the Examiner enter the foregoing amendment to the claims to place the application in better condition for allowance or

appeal. Applicant also requests that the Examiner reconsider the claims in view of the foregoing remarks.

It is believed that no fees are due in connection with this amendment. If any fee is due, please charge Deposit Account No. 08-2025.

Respectfully submitted,

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